Attorney Docket No. 10559-391001
Serial No.: 09/745,104
Amendment dated January 20, 2004
Reply to Office Action dated November 19, 2003

Amendments to the Specification:

Please replace the current title as follows:

A1

Hardware Loops and ~~/~~ Pipeline System Using Advanced Generation of Loop Parameters

Please replace the paragraph beginning at page 4, line 9 with the following amended paragraph:

A2

Processor 2 may include one or more pipelines 4 and a control unit 6. By way of example, the pipelines 4 may include one or more system pipelines, one or more data address generation pipelines, one or more execution unit pipelines, and one or more additional pipelines, as may be desired for a particular implementation. Control unit 6 may control the flow of instructions and/or data through the pipelines 4 during a clock cycle. For example, during the processing of an instruction, control unit 6 may direct the various components of the pipelines to decode the instruction and correctly perform the corresponding operation including, for example, writing the results back to memory.

Attorney Docket No. 10559-391001
Serial No.: 09/745,104
Amendment dated January 20, 2004
Reply to Office Action dated November 19, 2003

Please replace the paragraph beginning at page 11, line 1 with the following amended paragraph:

A3

The top and bottom values may indicate which instruction is at the top of the loop, and which instruction is at the bottom of the loop. The top and bottom values in the loop setup instruction, however, may be program counter (PC) relative. Therefore, a calculation (40) in AC stage may be used to obtain the top and bottom values that will be written to ETop 34A and EBot 34B registers respectively. After the loop setup instruction enters EX 1 (41), the top and bottom values may be written to the ETop 34A and EBot 34B registers (42).